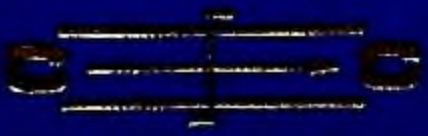
DIGITAL ELECTRONIC DESIGN
VOLUME 1

CATT, WALTON & DAVIDSON



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PREFACE

The authors have become increasingly concerned at the lack of clear and accurate information on many aspects of digital design, even though this fast growing discipline is the basis of the third largest industry in the U.S.A. They have decided to contribute towards remedying this situation by publishing a series of volumes which concentrate on those aspects of the subject which have been ignored or misunderstood.

The authors graduated from British colleges. They have a total of more than forty years of experience in Britain and the U.S.A. centred on digital design, and have published widely in the technical journals. They give seminars on digital design, and act as consultants to industry.

Also see "Electromagnetism 1" by Ivor Catt, pub. Westfields Press, 121 Westfields, St. Albans AL3 4JR, England, 1994.

Westfields Press also offer "Oliver Heaviside, The Man", a biography, and "Death of Electric Current", a reprint of many of the articles in Wireless World from 1974 to 1989.

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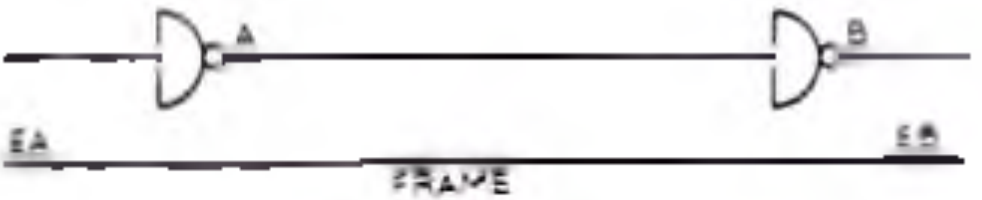
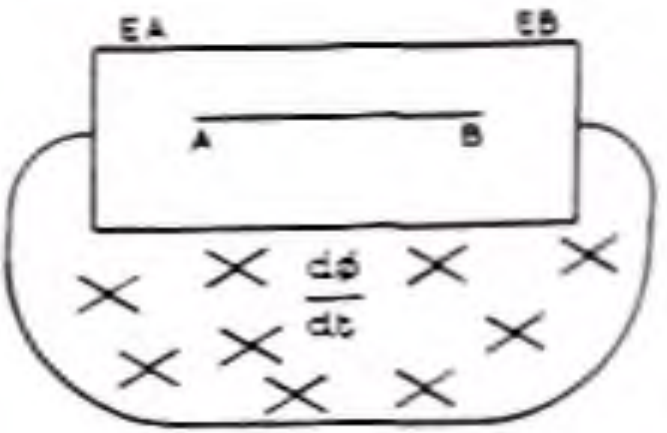
EARTHING IN A DIGITAL SYSTEM

Consider a signal line from A to B, carrying a logic signal which is referenced to the machine frame at each end.



The logic gate at A (which can be regarded as a voltage source with very low output impedance) puts the correct logic signal v between A and E_A. After a short delay, this signal arrives between B and E_B. Let us now consider the whole machine, and the line AB within it.



Let us suppose that the electrical interference causes a magnetic flux change $d\phi/dt$ to thread the loop formed by the frame of the machine and an earth loop, for example. By Lenz's Law, this will result in (an eddy) current flowing around the loop in such a way as to oppose the change of magnetic flux. It will pass along the frame from E_A to E_B, and some will pass down the signal line AB. (An alternative reason for a surge of current would be if a human who was charged up with electricity touched the end of the machine, and the current was discharged from the human down the frame of the machine.) Because of the non-zero destination impedance of the signal line at B, and also due to the difference in physical size etc. of lines AB and E_AE_B, the effect will not cancel out, and so the amplitude of the logic signal seen across BE_B will be affected. Clearly the more the reference line E_AE_B could be made to look like the signal line AB, the better would be the rejection of such interference.

One obvious improvement would be to separate the logic 0v from the machine frame as much as is possible (and legal. Safety considerations indicate that all circuits should be tied down to earth). So if it is possible, we turn the machine frame effectively into a screened room, and keep all the logic and reference (0v) inside as far from the frame as possible, except for the single link between 0v and frame for safety reasons, preferably at the point where the incoming mains earth is also connected to the frame. The screening effect is best if the capacitance between frame and the 0v grid is kept to a minimum. This indicates that the amount of 0v bussing should be kept down, a point which conflicts with the conventional wisdom on the subject of 'good grounding'. However, there is not really much chance of reducing the 0v to frame capacitance very much, once the obvious precaution has been taken of avoiding whole surfaces of 0v separated from surfaces of frame by only a few thousandths of an inch of insulation, and the total capacitance between 0v and frame throughout the machine is then down to around 1,000

picofarads or so. This represents about 200 ohms at 1 MHz, which is the kind of frequency at which we worry about externally induced interference. At this frequency therefore, if the 0v and frame are separated as much as is practicable, the impedance between the two is still only 200 ohms in a typical machine which is one or two metres long and high.

By moving the 0v and signal lines inside, as far as possible away from the frame, we have done as much as we can to ensure that externally induced interference flows down the frame only, leaving the logic unaffected. The next thing we can do is to consider whether we can nullify the effect of what little interference still does penetrate inside onto the 0v and signal lines.

Let us assume that a large current, caused by external interference, flows down the 0v bus. (We are thinking in terms of 1MHz noise, and not very high frequency noise like 100MHz. At 1 MHz, where the wavelength is 1000 feet, the picture shown in Figure 3 is valid. That is, the wavelength is long compared with circuit dimensions, and the machine frame is part of a loop as in Figure 3 rather than part of a

transmission line, as it would be at 100 MHz and above.)

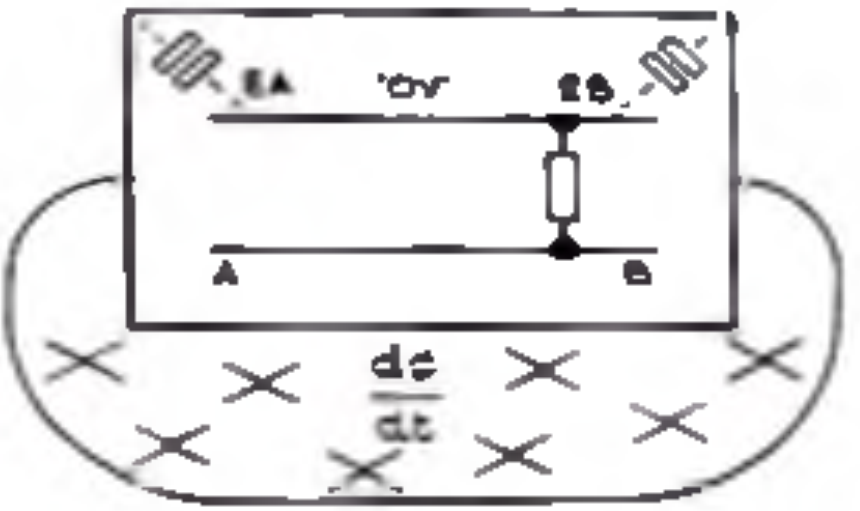
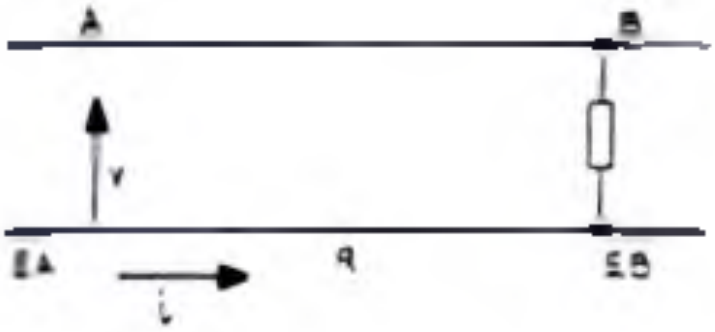


Figure 3

Due to resistance in the 0v line between E_A and E_B, there is a voltage drop between them. The source impedance AE_A can be neglected, since the circuit driving the logic signal output is a voltage source. But the impedance BE_B, the destination impedance, is large compared with line resistances, so very little of the current caused by external interference flows down the signal line. This means that there is no voltage drop down the signal line to cancel out the effect of the IR voltage drop between E_A and E_B due to the earth current caused by externally

induced current and the resistance of the earth line between E_A and E_B.



i = noise current
R = earth resistance
v = correct logic signal
v_{BE_B} = v + iR

The above is a rough and ready description of what is really a complex situation, but it is sufficient to illustrate the point, and to show why noise into the 0v line E_AE_B is not cancelled out, but upsets the magnitude of the logic signal at BE_B. The reason is that the path E_AABE_B is different from the direct path E_AE_B, the former being a high impedance path (due to R_{BE_B}) and the

latter being a low impedance path, so that the interference affects them differently.

It is worth pointing out in passing that if noise is magnetically induced as shown in Figure 2, it will be shared across the source E_AA, the line AB, and the destination (where it does the damage) BE_B proportionate to the three impedances. This means that a high source impedance R_{AE_A} will "soak up" more of the noise and keep it away from the destination. This contradicts the conventional view that a low output impedance for a logic gate is best for noise rejection. (However, capacitively induced noise will be best suppressed by a low output impedance.)

EARTHING IN A SYSTEM COMPRISING MORE THAN ONE MODULE

The best approach to a system with more than one module is to extend the technique discussed previously for a one-module system.

The frames of the modules are connected together to form an extended "screened room". Inside the frames, the 0v and the signal lines should be connected from one module to the other, keeping the capacitance to frame to a minimum. Notice that if the frames are connected together via a good shield around the interconnecting cable, the screening around the cable

may be best, but the capacitance between Ov and the screen (i.e. the frames) may be alarmingly high, perhaps 400 pF, or 400 ohms at 1MHz. It follows that the best screen may not be best for the system, which demands not only good screening by the frames, but also minimum capacitance between Ov and the screen. However, in practice this question turns out to be rather academic, because in any case it is hard to reduce the capacitance between Ov and screen in the interconnecting cable significantly. However, we try to counterbalance the tendency for Ov to be upset in the interconnecting cable by providing more noise rejection in signals going between modules than in signals within one module.

SAFETY IN A SYSTEM COMPRISING MORE THAN ONE MODULE

The reader may have noticed an anomaly in the above discussion. First, we say that the Ov grid should be kept as far as possible from frame, so that the frame will screen the logic from external electrical interference. Second, we concede that for reasons of safety, Ov and frame

must be tied together, so we rule that this should occur only once (although this has already marginally degraded the system, making it slightly more susceptible to interference. A completely floating electronics would be ideal from the point of view of noise rejection.) Now we are considering a system with more than one module. Should 0v and frame be connected together in only one module? If so, what happens to safety if two modules are disconnected, so that now one module's electronics has lost its earth strap?

The above is the first problem. The second problem arises if, as so often occurs, electrical power enters each module separately from outside. What do we do with the earth (third) wire coming into the second and third modules, and so on? Let us discuss these two problems separately.

CONNECTING 0v TO FRAME IN SYSTEMS COMPRISING MORE THAN ONE MODULE

From the electrical point of view, the ideal solution is to have 0v isolated from frame in every module except one, the main module. However, this is frightening from the point of

safety, since in most systems it is easy (and possibly necessary) to separate modules while still being able to supply power to them.

The worst possible situation arises if we try some sort of compromise, by tying 0v to frame once, and only once, in every module. This is worse than strapping 0v to frame everywhere, because there is a tendency for interference to be picked up by the frame (acting as an antenna) and then directed into specific areas of the logic. So if it is not possible to limit the number of connections between 0v and frame in the whole system to one, they should be connected everywhere, so that the frame becomes the basis of the 0v grid.

The reader might think that the latter course is the practical one in the circumstances, that is, to forget about trying to use the frame as a screen and revert to "good grounding techniques" by tying 0v to frame everywhere. However, he should be warned that the world is littered with systems where this has been done and where the performance is unsatisfactory - computers which keep failing for no apparent reason, or

which fail when someone touches them. (A discussion of the mechanism of electrostatic discharge when a human touches a machine and its effect is discussed elsewhere.) If a machine is to work really satisfactorily, this problem has to be faced. A multiple module system, being larger than a single module, picks up even more electrical interference that a single module. The only viable solution is to have 0v tied to frame only once in the whole system (unless the advice in the next paragraph is taken). The designer must also ensure that the current carrying capability of the 0v line between modules is sufficient to carry the current needed to blow a mains fuse in another module, should a fault occur in a subsidiary module so that there is a heavy surge of current into the 0v grid.

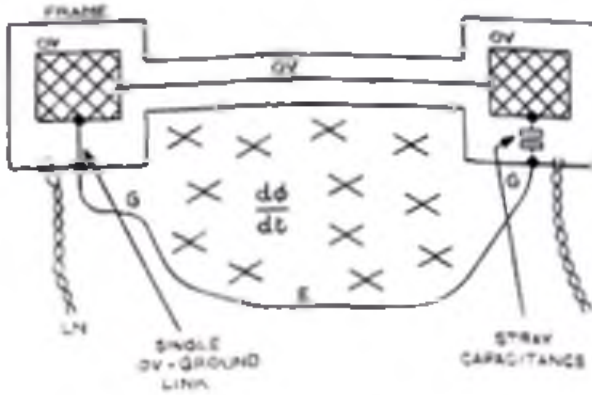
A good way out of this dilemma is to tie 0v to frame only through a choke (inductor). This is quite practicable. For instance, a 200 μH choke which will carry 20 amps weighs only a kilogram or so, is only 10 cm. cube in size, and costs around ten dollars.

SPECIFICATION OF 0v CHOKE. The choke must be able to carry a current

in excess of the rating of the mains fuses in the system, meaning something like 20 amps. Further, it should not saturate at this current, because in the case of a human touching the 0v line, and so discharging to earth through this choke, it should be able to absorb all of the energy stored in the electrostatic charge in the human before saturating, and so be effective in limiting the current and the rate of change of current through it, since the current causes troublesome iR drops across the 0v grid, and the changing current causes troublesome electromagnetic fields. These requirements are met by a 200 μH choke which saturates at 20 amps.

EARTH WIRES ENTERING MORE THAN ONE MODULE

If mains power is supplied individually to modules, and the earth (third) line is tied to the local frame every time, a second situation arises which causes designers some concern. This is because a complete loop is formed by the two earth lines and the frame. Should some stray magnetic flux $d\phi / dt$ happen to pass through this loop, then by Lenz's Law,



a current will flow around the loop which will tend to oppose this change of flux. Now we see the value of separating 0v from frame, so that this current only flows in the frame and does not get near the logic, except via stray capacitance between 0v and frame in module 2, which is kept as low as possible (say 1000pF, or 200 ohms at 1 MHz.) The path through the frame is very much preferred by this current over the high impedence path via the 0v grid, so that 0v throughout the system tends to stay at the same potential as the potential of the earthing point in Module One. (This

last remark is a practical approximation to the truth rather than the complete picture, which is complex.) So we see that the existence of the earth loop is not very serious. (However, if 0v had been tied to frame throughout the machine, it would be of much more concern, and the machine would be very susceptible to interference. This susceptibility could then be reduced by cutting all the earth lines into the machine except one, but here again we have a safety hazard.)

A good case can be made for the use of a choke to connect the earth line into the module frame. The discussion on values, cost and size is the same as in the case of the choke to connect 0v to frame, which has already been dealt with.

INTERFERENCE FROM 50 HERTZ MAINS

Single phase power is supplied by a cable comprising three lines, Live, Neutral and Earth (L, N and E). The Live and Neutral connect to the primary of one or more power transformers, and the Earth line is connected to the frame of the machine for safety.

Interference from the mains can be classified into three types:

1) Balanced. The noise signal travels equally down the L and N lines, and the E line acts as a return path. It is called Balanced by electrical power engineers, and would be called Common Mode noise by electronic engineers. Balanced noise was the mains - borne interference of most concern in wireless telegraphy and other electronic activities which preceded digital electronics. It caused "earth currents" which would upset high gain linear amplifiers.

2) Unbalanced. The noise signal travels down the L line and back on the N line, leaving the E line

unaffected. It is called Unbalanced by electrical power engineers, and would be called Differential Mode Noise by electronic engineers. Unbalanced noise was not of such concern in the past, because it tended to get lost (i.e. suppressed) in the D.C. power supply. It can be shown that any complex signal travelling down the three lines L, N and E, can be resolved into a Common Mode component and a Differential Mode component.

3) Mainsborne radiated noise, both Balanced and Unbalanced. The noise enters the module frame via the L, N and E lines, where it then radiates directly into the logic.

SUSCEPTIBILITY OF A DIGITAL SYSTEM TO MAINS NOISE

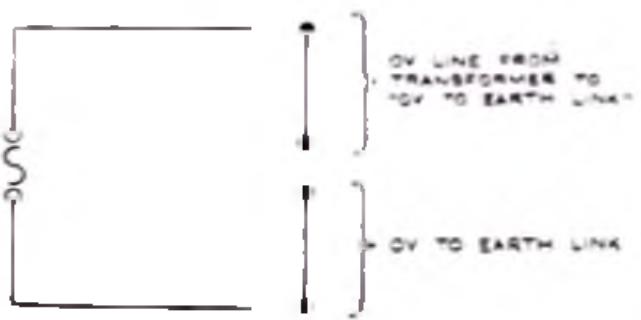
Differential mode noise on the L and N lines tends to be smoothed out at two points, both at the Rough D.C. capacitors and also at the Regulated D.C. capacitors. However, large value capacitors have significant "series inductance" because of long connecting leads, so that some of the noise, if not suppressed before the transformer primary, will pass all the way through the power supply and cause transient

TO LOGIC
REGULATED D.C.
0V
SERIES REGULATOR
ROUGH D.C.
0V
STRAY INTER-WINDING CAPACITANCE
L
N

variations of the logic power supplies which will tend to disrupt the correct operation of the logic. Screening the transformer will not help significantly, because at the frequencies we are most concerned about, in the region of 1 MHz, differential noise is fed through the transformer from primary to secondary by transformer effect, not via inter-winding capacitance.

Common mode noise gets through the transformer via inter - winding capacitance, so a screened transformer will very much help to suppress common mode noise at a very reasonable cost. (Typically, inter-winding capacitance for an unscreened transformer is 100 pF. With screening, this falls to an effective 1 pF or so in the region of 1 MHz. At 1 MHz, 1 pF looks like an impedance of about 200 Kohms.) Otherwise, what noise does get through the transformer will tend to lift the +ve voltage relative to 0v and Earth, and it will tend to lift the level of 0v at some points on the 0v grid compared with others. The use of a choke rather than a short in the safety link between 0v and Earth will of course help to render the logic immune to this noise, because all the logic will tend to move together. Another way of

putting this is to say that common mode noise which <u>does</u> find its way through the regulated D.C. lines will then see three loads in series; the link between the E line and frame, the link between frame and Ov, and the line carrying Ov across the logic to the link. If the Ov to frame to E line link has a high impedance (i.e. is a choke), most of the noise will appear harmlessly across it. The D.C. resistance of the choke should be kept below the maximum allowed by the electrical safety standards. (B.S. 3861 section 6 indicates that the D.C. resistance of such a choke should be less than 0.1 ohms.)

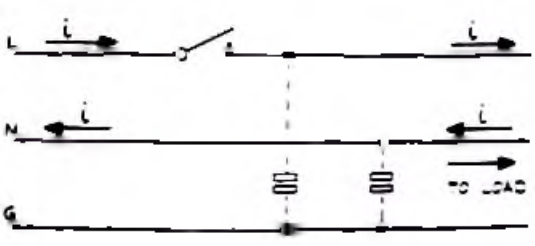


However, if the Ov to E link is low impedance, the impressed noise will devote itself to lifting the potential at one point of the Ov grid compared with the potential at another. This, of course, will degrade the logic signals, and tend to cause system malfunction.

Mainsborne radiated noise, which is radiated from the mains wires inside the module, is greatly reduced by screening the L and N lines, the screens being earthed to the machine frame. Since screened cable is awkward to handle, it may be wise to try to avoid it. This can be done by having the mains filter at the point where the power line enters the module, so that the mains lines within the module will be smoothed, and screening can be avoided. Another approach is to have mains lines in the module separated from the vulnerable logic by properly earthed bulkheads. Once past the mains filter, the mains cables need not be screened in normal circumstances. (That is, so long as power is never switched on and off to certain loads within the module, for instance compressors, while the logic is operating, switching transients in the mains should definitely be screened from the logic.)

MAGNITUDE OF MAINS BORNE INTERFERENCE

A reasonable noise amplitude to design against in a 240 volt single phase supply is 2 Kvolt over the range of 100 KHz to 10 MHz. (When thinking of the problem, imagine a pulse 2Kvolt high with a 1 μsec loading edge and 10 μsec width.) The noise may be common mode (down L and N and back on E) or differential mode (down L and back on N). It might be caused by the switching off of a 1 H.P. motor somewhere else on the same supply. When the switch is broken, there is a massive inductive kick from the load (motor windings) as it tries to maintain the current. This may pull current out of the E line via the capacitance between E and L. There will also be arcing (flashover) between the switch contacts, and so a complex voltage waveform results.



It is wise to assume large amplitude noise; definitely more than the nominal 240 volts of the line, and also it is wise to assume both common mode and differential mode noise.

The source impedance of the noise is difficult to determine. It is safest to assume a very low source impedance, say 2 ohms. Both this conservative assumption, and also the assumption that the noise has an amplitude of 2 Kvolt, which might surprise the reader, since this is something approaching an order of magnitude more than the nominal mains voltage, do not present the designer with a problem which is very different from the one he would have to face if he optimistically assumed a maximum noise equal to the nominal peak mains value, about 350 volts, and a 50 ohm source impedance, so he may as well play safe.

Useful confirmation of some key information in this chapter is found in "Transient Voltage Suppression Manual" by General Electric Semiconductor Products Department, 1976.

FILTERING THE MAINS

Mains filters are made up of capacitors and inductors.

1) Capacitors. Those connected to the L line have 240 volts across them, and so need to be rated for 240 volts 50 Hertz. They have to be able to dissipate the heat resulting from a rather surprisingly large current.

By Ohm's Law, $V = I Z$

$$I = \frac{V}{Z} = \frac{V}{1/6\pi C}$$

$$= 240 \cdot 300 \cdot C$$

For a reasonable value of capacitance, 1 μF, we find that the current turns out to be something approaching one tenth of an amp. It is surprising to realize that a mains filter can significantly alter the power factor of a load.

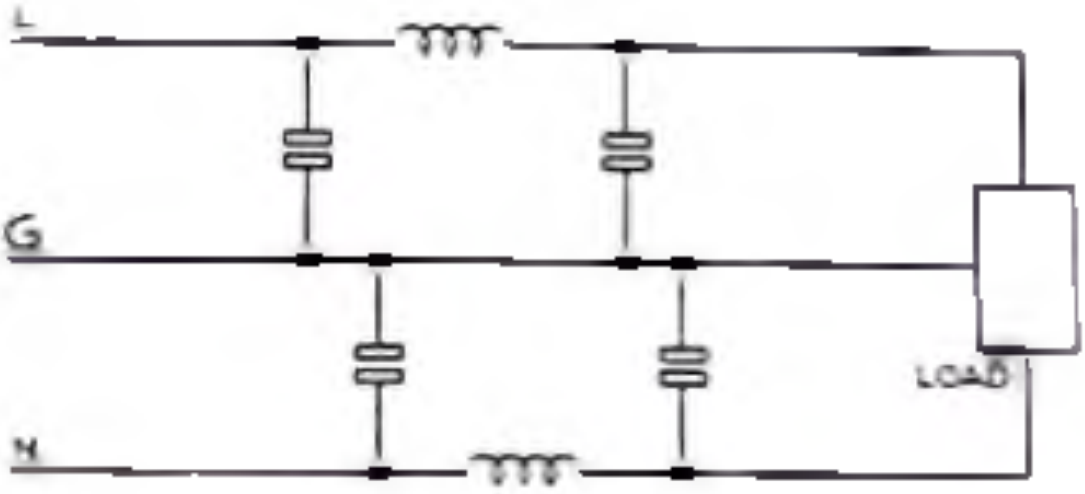
The series inductance of such a capacitor, which incidentally is less than one cubic inch in volume, can be as low as 10 nH, which is very satisfactory for our purpose. (At 1 MHz, 10 nH has an impedance of around 50 milliohms.)

2) Inductors (Chokes). The important thing is to make sure that even at peak current the inductor is not saturated. If the power taken by the module is around 1 KW, so that the r.m.s. (measured) current is around 4 amps, the peak current may be as high as 10 amps. Noise must be suppressed during this peak current as much as at any other time.

A choke which saturates at 20 amps and has an inductance of 200 μH costs something like twenty dollars and is about ten cm. cube in volume. Its parasitic capacitance can be as low as 10 pF, which is very satisfactory for our purpose. (At 1 MHz, the impedance of 10 pF is around 20 Kohms.) The D.C. resistance of such a choke is around 0.1 ohms, so it will be possible to meet safety requirements should the choke be put in the earth line. (In Britain, B.S. 3861 section 6a.)

TYPES OF MAINS FILTERS

A mains filter is a low pass filter; that is, it allows through low frequencies but blocks high frequencies. It contains series inductors and parallel capacitors. The usual circuit is a double π



High frequency signals entering on either the L or N lines see a high impedance inductance ahead and are shunted to earth through a low impedance capacitor. Typically, at 1 MHz, with C = 1 μF and L = 200 μH,

$$Z_C \approx 0.2 \text{ ohms}$$

$$Z_L \approx 1 \text{ Kohms}$$

If the source impedance of the noise is 1 Kohms or higher, this attenuates the noise by a factor of

$$\frac{1 \text{ Kohm}}{0.2 \text{ ohm}} = 5{,}000$$

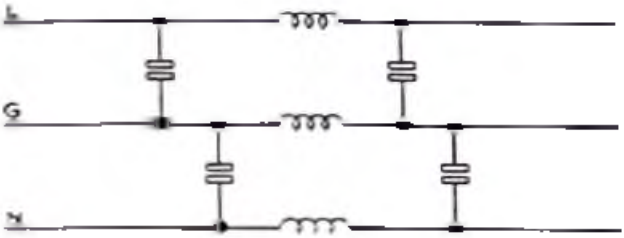
or about 70 db.

If the source impedance of the noise is low, the first capacitor is ineffective, but the potential divider

by the inductor and the second (downstream) capacitor still give around 70 db attenuation at 1 MHz, regardless of the impedance of the load.

DISCUSSION OF THE ABOVE CIRCUIT

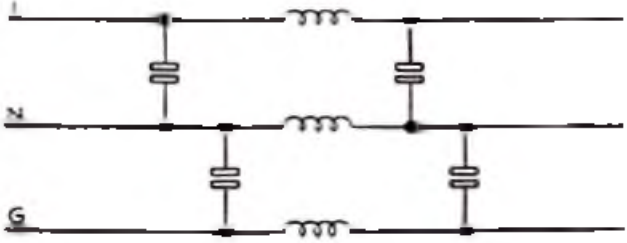
The filter is reassuring because it appears "safe". Any high frequency signal approaching from either direction sees a short to earth, which seems to shunt away the noise, and also sees a high impedance series inductor blocking its path ahead. If we were only worrying about noise coming down the mains, it would be fine. However, it effectively clamps all the lines, both input and output, together at high frequency, so that the "earth loop" pickup of externally radiated noise, see page 21, can now also result from an L or an N loop, and so looks much more likely. Also, the possibility of electrostatic discharge into the module seems much more likely. From the point of view of radiated noise, the following circuit, which blocks the passage of high frequency signals down any lines, seems preferable. It makes the path down these lines an open circuit to high frequencies, and tends to isolate



the system completely from its environment.

EARTH CURRENT

The above filter causes a disquieting amount of earth current. If the capacitors are 1 μF, the total earth current is about 150 ma. It seems much preferable to re-arrange the lines as follows:



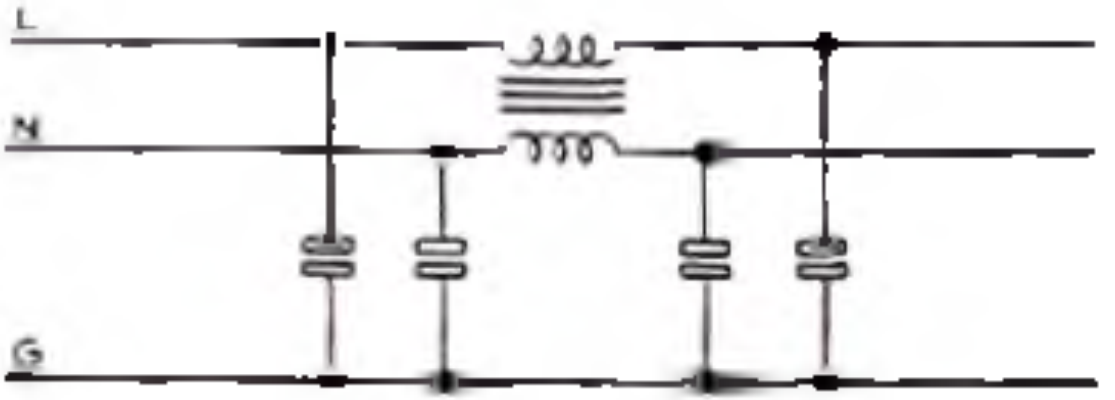
The noise suppression is very little altered (being slightly improved for differential mode noise and slightly degraded for common mode noise), and the earth current is reduced to a negligible amount, perhaps 2 ma. The circuit seems much safer too, because there are now no components linking L directly to E. This means that a single shorted capacitor presents no possibility of a safety hazard.

MAINS FILTERS ON THE MARKET

There are basically three types of filter on the market; the cheap (20 dollars), the medium performance (100 dollars) and the high performance (400 dollars). The medium performance filters have about the right kind of specification - around 60 db insertion loss in the region of 1 MHz. A filter meeting this specification would cause 2 Kvolts of noise to be reduced to a mere 2 volts, which latter would easily get lost on its way through the power supply. The high performance filters, specified at 100 db insertion loss, reduce noise of 2 Kvolts down to an unnecessarily low 20 mv.

The weak point in the above analysis is the assumption that the filters meet the manufacturers'

specifications. The most serious shortcoming is when the windings of both chokes are on the same core. The idea is that the currents in the L and N lines, being equal and opposite, create zero total magnetic flux in the choke.



This means that for a heavy L and N current, the core will not saturate, and a single toroid costing one dollar can be used in place of two separate chokes costing twenty dollars each. Of course, instead of two chokes we now have merely a transformer, which will not stop differential mode noise at all. Unfortunately, even if the 50 ohm insertion loss is only 10 db for differential mode noise (down on L and back on N), manufacturers of such

filters still feel entitled to claim 60 db insertion loss, leaving the unlucky customer to falsely assume that they claim this performance for differential mode noise as well as for common mode noise. The author has never seen a manufacturer's specification where insertion losses for both differential (unbalanced) mode and common (balanced) mode noise were unambiguously defined. Further, 50 ohm insertion loss means the ratio of the amplitude of the output from the filter into a 50 ohm load divided by the input from a source with 50 ohm source impedance.

Sometimes, the manufacturer gives the 150 ohm insertion loss instead. However, usually he does not tell you

what Insertion loss it is, but merely presents you with a single graph without explanation. Since both the source impedance of the noise is difficult to determine, and the impedance of a load, certainly the instantaneous impedance (of a bridge rectifier for instance,) is virtually impossible to determine, the proper filter performance to specify is the "Minimum Insertion Loss", that is, the worst case (least) attenuation when the source impedance and load impedance are independently varied from zero ohms to infinity.

For availability of improved filters, send s.a.e. to the publishers of this book.

DISTRIBUTION OF D.C. POWER TO LOGIC

In a digital system, sudden massive changes of load current in the power supply serving the logic can easily occur. For instance, it is not uncommon for a 32 bit word of data to be gated onto 32 parallel signal lines. If the word happens to be "all ones", the amount of current suddenly switched out of the +5 volt supply is quite large. For instance, if the lines are shunt terminated in their characteristic impedance of 100 ohms, the total current switched, at 50 ma per line for a 5 volt signal, is 1.6 amps. We see what a massive event this is when we assume a reasonable rise time for the signal, say 5 nsec, and find that the rate of change of current out of the supply,

$$\frac{di}{dt} = \frac{1.6}{5n} \text{ amps/sec} = 320 \text{ million amps/sec}$$

For proper functioning of the logic it is important that such a massive, rapid current demand should not cause

a significant drop in the voltage bus in the vicinity of the demand at any time after that demand has occurred. (A 50 mvolt drop could be regarded as the maximum acceptable.)

A hierarchy of energy reservoirs, or capacitors, sustains the D.C. voltage at the critical point. During the first few nanoseconds, a small capacitor, near to the point of the suddenly changing load, supplies the current. Later, other similar capacitors distributed around the logic a little further away help out. Later still, when all the small local capacitors would have been depleted, the larger energy reservoir of (say) 20,000 uf in the power supply itself sustains the voltage.

As this final reservoir begins to be depleted, the series pass transistors in the power supply alter their current level to supply the deficiency.

The diagram on the next page shows a typical hierarchy of energy stores such as might be found in a system in use today. At every stage it is deficient. Starting at the right, each capacitor has to have become seriously depleted, its voltage dropping by a volt or two (compared with the maximum

LOAD
1·6 AMPS
400nH
1µF
ON PLUG IN BOARD
2µH
100 × 1µF
ON NEARBY BOARDS
20,000 µF IN PSU
20 KHz BANDWIDTH
RAW D.C.

reasonable drop of 50 mv) before there is enough voltage and time developed across the next inductor to the left to cause it to pass the required increase of 1.6 amps. The situation is unsatisfactory by orders of magnitude, showing that it is not merely some systems that are deficient. In fact, most systems in service today are unable to supply a perfectly normal change in current demand at one point in the system while keeping the D.C. voltage bus near to its nominal value.

Why do systems continue to function if the above assertions are true? The answer is that an important element in the total picture was omitted from the diagram, and that was the other steady loads. When the 1.6 amps is switched on, the D.C. voltage supply begins to sag. The result is that, with a reduced voltage across them, the other circuits demand less current. If the D.C. voltage supply drops by 5%, the current taken by an integrated circuit falls by even more than 5%. (The current drop is more than linear with voltage because some of the available voltage is "lost" in fixed transistor V_{be} drops. This means that if there is

a 5% drop in the full voltage, the percentage drop across resistors in the circuit is more than 5%.)

If the full system load is 30 amps, a further load of 1.6 amps only calls for the removal of about 5% from this standing load, which is probably achieved by a drop of only some 3% in the D.C. voltage supply; a mere 150 mv in the case of a 5 volt supply. So we see that in a traditionally designed system, the voltage supply decoupling capacitors are to quite a degree merely a gesture of intent, and the real voltage decoupling is by the steady loads. This is unsatisfactory, because any change in D.C. voltage levels leads to a degradation of performance and possible failure. Timing circuits are upset, and margins against other types of noise are reduced.

When the 1.6 amps load is suddenly switched off, a similar problem arises. This time, the voltage bus rises above its correct value in order to repel the now unwanted current which continues to arrive. The amount of over-voltage developed is about equal to the amount of under-voltage

which occurred in the previous case. As before, the real voltage decoupling (or stabilization) in traditionally built systems is caused by the other steady loads, which start to take more current when the voltage across them increases.

The designer should make a conservative (that is, large) estimate of the maximum change of load that can be expected in the logic, and design a hierarchy of energy stores that can sustain such a load.

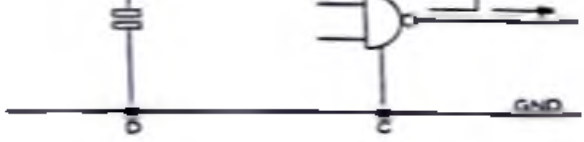
PRINTED CIRCUIT BOARD LAYOUT FOR HIGH SPEED SCHOTTKY T.T.L.

This subject is not a difficult one; indeed, the mathematics employed is extremely elementary. The problems are caused rather by the historical progression from analogue to digital techniques, with the consequent carrying over of well-tried analogue techniques into the digital environment. Unfortunately, the requirements for digital circuitry are frequently opposite to those needed by the analogue variety, and hence there is a need for a complete reconsideration of the requirements.

LOW INDUCTANCE BUSSING

To understand the criteria which determine how the +5v and 0v lines should be distributed to the t.t.l., first take the case of a t.t.l. gate driving its output line from low to high. For the gate to drive the output line high it must pass current into

it. The output line must be considered as a transmission line of impedance Z_o if its length exceeds 10 cm. In practice, Z_o will be in the region of 100 ohms, and for a single logic signal changing from low to high the instantaneous output current will be given by $I_o = 5/100 = 50$ ma. This current must be obtained from the supply rails in a time comparable to the rise time of the signal. If, for Schottky t.t.l., $t_{r(min)} \simeq 1.5$ nsec., then charge must be transferred from the decoupling capacitor to the gate and hence to the output line in this time. Remember that charge is obstructed from flowing into the gate by the inductance, L, of the loop ABCD in the diagram. If this is approximately 2cm square with reasonable track



width, then, using the formula for parallel wires,

$$L = \frac{\mu_o}{4} \ln \frac{a}{r}$$

$$\approx 30 \text{ nH}$$

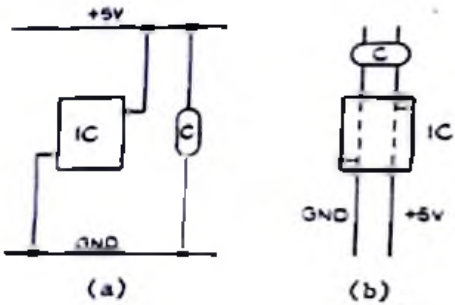
The e.m.f. dropped across L will then be given by $E = -L\, di/dt$. Therefore,

$$E = \frac{30 \times 10^{-9} \times 50 \times 10^{-3}}{1.5 \times 10^{-9}}$$

$$= 1 \text{ volt}$$

This is a considerable voltage, and it should be remembered that it is the result of a single gate switching. If all four gates in a pack switch together, the currents will be additive, and the rail will fall by 4 volts.

The first requirement of a power distribution system must therefore be low inductance between the i.c. and the decoupling capacitor. This is achieved by the track layout shown on the next page, where a low inductance path from C to the i.c. is provided by keeping the +5v and 0v tracks close together.



Manufacturers of i.c.s usually specify one decoupling capacitor for every 5 - 10 i.c.s which, with the track layout shown on the left above (a), results in prohibitively high inductance between the capacitor and the worst-case positioned i.c. The safest course is to provide the track layout as on the right above (b), but also to put one capacitor adjacent to each i.c. Clearly, this can be achieved by having one capacitor for each pair of i.c.s.

DECOUPLING CAPACITORS

The foregoing argument shows that the capacitor is better thought of as a reservoir capacitor which supplies

the local, instantaneous current which it can supply. Some manufacturers specify capacitors for i.c. decoupling by giving the maximum pulse risetime, which corresponds to a maximum current for a given size of capacitor. For instance, a 47 nF capacitor specified at 50V/μs can supply a current given by

$$i = C \frac{dv}{dt} = 47 \times 10^{-9} \times \frac{50}{10^{-6}}$$

$$= 2.5A,$$

which is adequate in the context of the previous calculation.

The other check to make is that the current drawn from the capacitor does not cause its voltage and hence the rail voltage to fall excessively. If the local demand is equal to ten gates switching, the current demand will be 500 mA; to be safe, assume that this demand lasts for 10 ns, and design for a voltage drop at the capacitor of 50 mV.

Thus, $$i = C \frac{dv}{dt}$$

$$0.5 = C \frac{50 \times 10^{-3}}{10 \times 10^{-9}}$$

$$C = 100 \text{ nF}.$$

This suggests that we should provide approximately 100 nF for each pair of packages.

It might be thought that radio frequency type capacitors are necessary for t.t.l. decoupling, but this is not so. To show why will be explained in a later volume. Briefly, it is because the frequently adopted model of a capacitor, which proposes that it possesses a lumped series inductance, breaks down in the case of a single applied step. There is therefore no reason for the designer to be afraid to employ non - ceramic capacitors. 1 μF tantalum beads perform well as decoupling capacitors.

TRANSMISSION-LINE MODEL

The best way to think of the power distribution system is as a transmission line, with each package connected to an ideal voltage source via an impedance equal to the transmission line impedance. (A package at the centre of a power bus will see two transmission lines in parallel and hence half the impedance. We will adopt the worse figure for the purpose of this argument.) This impedance must

be sufficiently low for negligible voltage transients to be produced on the line by gates switching within the package. The impedance of a transmission line is given by $Z_o = \sqrt{L/C}$ where L and C are the inductance and capacitance per unit length respectively. To calculate Z_o for the case of two tracks close together:

$$L = \frac{\mu_o}{\pi} \ln \frac{a}{r}$$

a and r are taken as 2 mm and 0.5 mm. Therefore

$$L = 0.6 \ \mu H/m.$$

If a 100 nF capacitor is placed every 5 cm along this line, then:

$$C = 100 \times 20 \ nF \ m^{-1} = 2 \ uF \ m^{-1}$$

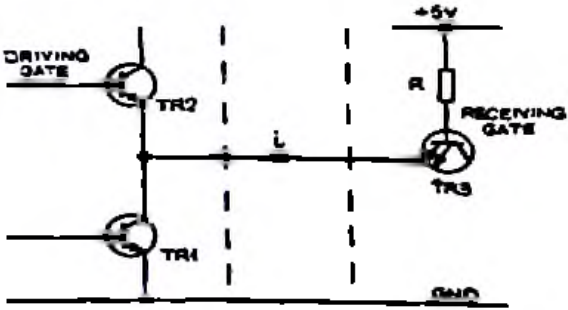
Therefore $Z \simeq 0.5$ ohms.

An instantaneous current demand of 200 mA - corresponding to four gates switching - will produce a voltage transient of 100 mV. This is only just acceptable, and suggests that the value of C should be increased. Note however, that laying out the tracks

with wider spacing and using smaller capacitors - 10nF for every few i.c.s, which is not uncommon, will create a situation much worse than this.

AUTO-DECOUPLING IN T.T.L.

In the context of the preceding remarks, some readers may wonder how systems which they have seen or have worked with managed to function at all, since it is common to see most or all of the above design guidelines violated. To see the answer to this, consider the structure of the t.t.l. gate output circuit, when this is driving the following gate input low:



According to the specification for, say, a 7400, the typical values of I and R are 1.0 mA and 4 kohms respectively. When the gate output is low it sinks a current i, given by:

$$i = \frac{(V_{cc} - V_{be} - V_{ce_{sat}})}{R}$$

where V_{be} is the base-emitter voltage of Tr_3 and $V_{ce_{sat}}$ is the collector saturation voltage of Tr_1.

If V_{be} and $V_{ce_{sat}}$ = 0.7 volts, to take a worst-case example, and

$$V_{cc} = 5 \text{ volts}$$

$$\text{then} \quad i = \frac{3.6}{R}$$

Now consider what happens if the rail voltage drops, due to a transient load imposed by the output of another gate switching. When V_{cc} drops, there is (to a good approximation) no change in the V_{be} drops. Suppose the rail

drops by 10%. Then:

$$i_1 = \frac{5 - 1.4}{R}$$

$$i_2 = \frac{4.5 - 1.4}{R}$$

Therefore

$$\frac{i_1 - i_2}{i_1} = \frac{0.5}{3.6} = 14\%$$

In other words, a 10% change in V_{cc} produces a 14% change in the current load placed on the rail. In effect, what is happening is that each gate output which is holding another input low acts as a 'reservoir' of current, and when the rail voltage drops as another gate drives its output high all the other gates give up some of their current to assist. This is what one would call the 'good neighbourliness' effect in t.t.l. In general, some gates on a voltage bus will be low and so act as current supplies. The problem arises when none or only a few are in this state - a critical situation for a badly designed system and one which could cause failure. It should be

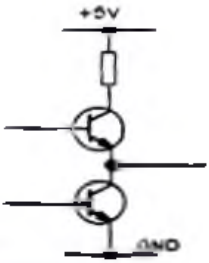
remembered that a logic system should work for all possible combinations of states which can occur in practice, and a hazard of this type could have serious consequences. It is therefore insufficient to demonstrate that a system 'works', because if the power distribution system is badly designed there is always the chance of an untested situation bringing about a failure of the system. It is assumed that in a logic system of reasonable size it is impossible to test all possible combinational situations, and doubly impossible to test all possible changes of situation!

The problem with Schottky t.t.l. is that the increase in speed does not allow time for the 'good neighbourliness effect' to act; consequently one is many times worse off with Schottky than with ordinary t.t.l. Schottky is a less forgiving family than conventional t.t.l., and much more care must therefore be taken with power distribution to ensure reliable performance.

THE CURRENT SPIKE

As just described, the main cause of transient current demands in a

Schottky t.t.l. system is the initial current surge when a gate switches into its transmission line load. The manufacturers' data overlooks the mechanism entirely. There is another cause of transient current demand which results from the 'push-pull' design of the t.t.l. output stage below.



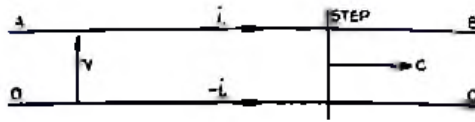
The current spike is produced because, on the 0 to 1 transition, the upper transistor turns on while the lower transistor is still turning off. This leads to a current surge of 10 mA with duration of about 10 ns. (See Bonham, B. 'Schottky t.t.l.', T.I. application report B93.) Provided the design guidelines laid down in the earlier sections with regard to power

supply bussing and decoupling have been followed, this small additional hazard will be taken care of. In fact, since a logic gate is driving a transmission line which is a resistive rather than a capacitive load, there is no need to provide a totem pole output, and this must be regarded as one of the bad fentures of the t.t.l. family.

INTERCONNEXIONS

To implement a system successfully using the t.t.l. family it is necessary to interconnect correctly between logic gates.

TRANSMISSION LINES. The correct model to use for interconnexion between logic gates is a two-wire transmission line. It is impossible to understand how a signal travels from gate to gate without taking the return path into consideration. Indeed it is impossible for a signal to travel without a return path! Consider the two-wire transmission line shown on the next page, in which a zero rise-time is propagating to the right with velocity ©. Ahead of the step there is no current in the wires and no voltage



differences between them. Behind the step there is a current i in the direction of AB and a current -i in the direction of DC with a voltage difference V between the wires. It can be shown that $V = iZ_o$,

where $Z_o = \sqrt{\frac{L}{C}} = \sqrt{\frac{\mu}{\epsilon}}$

where Z_o - characteristic impedance of the line,

L = inductance per unit length of the line,

C = capacitance per unit length of the line,

μ = permeability of medium between the wires,

ϵ = permittivity of medium between the wires.

The velocity of propagation © is

$$© = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{\mu\epsilon}}$$

These equations are true for any two - conductor system where the resistance of the conductors can be neglected and the medium between the conductors is well - behaved. These

conditions are met by tracks on a printed circuit board for any track width which can be manufactured. The step which we have just described is a transverse electromagnetic disturbance. Since the equation relating current and voltage on a transmission line is $V = IZ_o$, it follows that the effect of a transmission line on the driving circuit can be considered in terms of a resistance $R = Z_o$ connected in place of the line. This was the procedure followed earlier in calculating the current drawn from the supply rail by a gate as it switches.

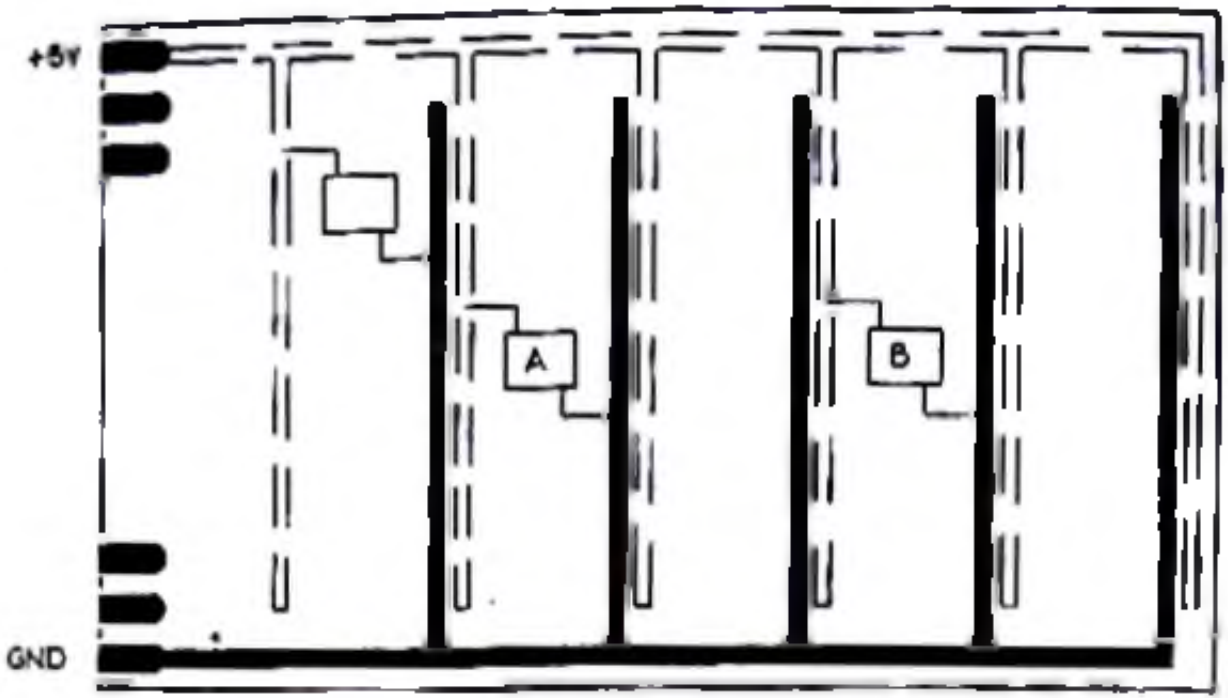
The impedance Z_o depends on the cross-sectional geometry of the conductors employed, and it is very difficult to calculate except for very simple cases. It is, however, a relatively slowly varying function of the geometry (usually logarithmic; see Gunston, M.A.R. 'Microwave transmission line impedance data', Van Nostrand Reinhold,) and therefore need not worry us too much. For a track on a printed circuit board laid out according to the design rules evolved in this paper, a value of Z_o of around 150 ohms can be assumed.

One key feature of a board of logic which distinguishes it from most analogue systems is that there are a multiplicity of signal paths from various points scattered about the board to various other similar points. It is essential that each of these signal routes has an adjacent return path. The simplest way, conceptually, to achieve this is to provide a ground plane on one side of the board. In practice this is difficult since it usually requires multi - layer construction, with the increased cost and complexity which this entails, in order to accomodate the signal interconnexions. With Schottky t.t.l. it is not necessary to go to this extreme; all that is required is a ground grid laid out so that a signal line is never more than one inch away from its return path.

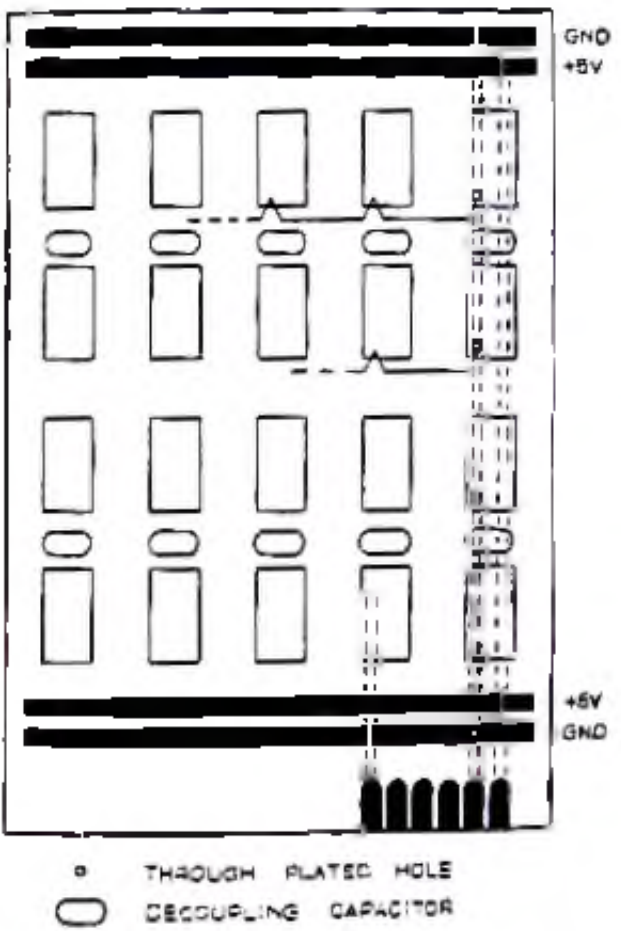
GROUND LOOPS. It might be argued that this scheme leads to ground loops which, from our experience with analog systems (e.g. audio equipment), are to be avoided. The plain fact is though, that on a logic board, ground loops are of no importance. The reasons for this are somewhat complex, but it is

probably useful to note one simple argument. In a high - gain amplifier, induction of a few millivolts at the input due to ground loop pickup can lead to an output of the same order as the signal. In logic this is not the case; a few millivolts into a gate input make no difference whatsoever. Hundreds of millivolts of noise are required before we will significantly degrade the noise immunity of a t.t.l. system.

It is probably valuable to examine a situation where a logic board has been laid out in order to avoid ground loops. A possible layout of power and ground connexions, which is quite common in the industry, is shown on the next page. Now, if circuit A sends a step to circuit B there is no adjacent return path. In practice, since a fast step requires a return path, it will simply use adjacent signal lines as returns, resulting in the induction of transient noise on these other signal lines. A further consequence is that the input to B will take a longer time to settle with a consequent reduction in the speed of the system. As was explained earlier, the layout shown on the next page is



A BAD LAYOUT GIVING HIGH INDUCTANCE AND FEW ADJACENT SIGNAL RETURN PATHS, WHICH LEADS TO CROSS - TALK


GND
+5V
+5V
GND
THROUGH PLATED HOLE
DECOUPLING CAPACITOR

also bad from the point of view of placing excessive inductance in the way of charge travelling between i.c.s and decoupling capacitors.

RECOMMENDED LAYOUT

A recommended scheme for laying out a printed circuit board is shown on the previous page. The power rails are run as near together as possible along the columns of integrated circuit packages and are interconnected at the top and bottom of the board. These provide return paths for logic signals travelling parallel to them. To provide return paths for signals travelling across the board, the ground pins of the packages are connected together from left to right. (Also consider connecting the +5 volt pins of the packages together from left to right.) This track, of the same thickness used for signal interconnexions, can be used for this. A tantalum bead 10 µF decoupling capacitor is provided between each pair of i.c.s. Notice also that ground connexions are brought out at regular intervals across the edge connector. These provide return paths for signals

travelling on and off the board.

If all these design rules are followed a reliable system will result and the consequent savings in servicing and testing will amply repay a little consideration given to board layout at the design stage.

Note in 1986, by I Catt.

I do not agree with the last page as to number of capacitors. Far fewer capacitors than one for each pair of I.C.s can be used.

THE INTERCONNECTION OF LOGIC

A logic system is composed of logic gates and interconnections between them. It is important, in order to ensure the correct functioning of the system, that an adequate model of this connection is used.

The simplest case is that of a logic gate driving another single gate, i.e. there is no fanout. We will return to the case of fanout in a later section.

It is impossible to consider the interconnection in the absence of a ground (or V_{cc}) return path. When this

In present we have both distributed capacitance and distributed inductance or, in other words, a <u>transmission line</u>. Thus the appropriate model of interconnection between two gates is a transmission line.

PROPERTIES OF A TRANSMISSION LINE

In order to discover how we characterise a transmission line we will consider a step propagating along a two-wire line.

Use Faraday's Law ($V = -\frac{d\phi}{dt}$) around the loop ABCD.
Define L as the inductance per unit length of the wire pair.

Then $L = \frac{\phi}{i}$ (1)

In a time δt, the step will advance a distance δs, such that,

$$\frac{\delta s}{\delta t} = \copyright \qquad (2)$$

and the change of flux will be,

$$\delta\emptyset = L\ \delta s\ i \qquad (3) - \text{from } (1)$$

Substitution into Faraday's Law gives voltage applied to line to overcome back e.m.f.

$$v_{AD} = L\ i\ \frac{ds}{dt} = L\ i\ \copyright \qquad (4)$$

Now we also obtain, from definition of a capacitor $q = vC$,

$$i = v\ C\ \copyright \qquad (5)$$

where C is the capacitance per unit length of the wire pair.
It now follows that

$$\copyright = \pm\ \frac{1}{\sqrt{LC}} \qquad (6)$$

and also $\frac{v}{i} = Z_o = \sqrt{\frac{L}{C}}$ (7)

Thus we see that such a step may propagate in either the x or -x directions. The two parameters which characterise a transmission line are the velocity of propagation © and the impedance Z_o, which relates the voltage difference across the line to the current in the line by an 'Ohm's Law' type relation,

$$v = i Z_o \qquad (8)$$

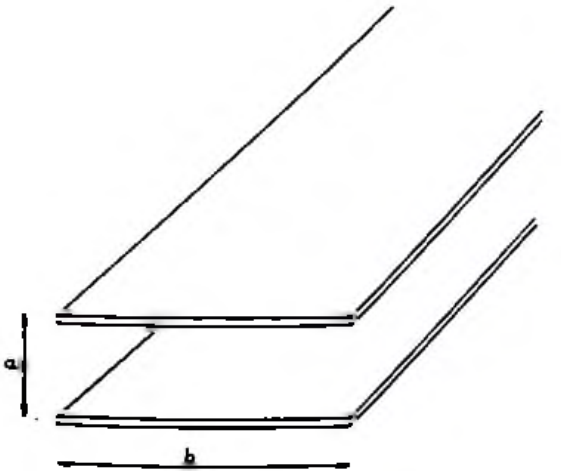
where Z_o is just a property of the geometry and μ and ϵ for the medium in which the wires are embedded. This will now be shown.

It should be noted that the above argument is independent of the idea of frequency, and Z_o and © do not depend on frequency provided μ and ϵ are frequency-independent, as they are in practice.

In order to use the formulae for Z_o and © we must have methods for determining L and C for any geometry we might be using. In general it will be impossible to solve analytically for L and C and so other methods must be resorted to.

THE ANALOGY BETWEEN L, C AND R

In this section we develop a useful analogy which leads to simplified calculation in all cases and to a simple technique of measurement in those cases which do not yield to calculation.
We will consider the special case of a parallel-plate transmission line.



We will calculate the resistance, capacitance, and inductance per unit length of the line.

RESISTANCE. If the medium between the plates has resistivity ρ, then the resistance between the plates per unit length is

$$R_1 = \frac{a}{b}\rho\frac{1}{f} \qquad (9)$$

where we have defined $\frac{b}{a} = f$ as a geometrical factor which is a dimensionless function of the dimensions of the line.

CAPACITANCE. For a parallel plate capacitor

$$C_1 = \epsilon\frac{b}{a} = \epsilon f \qquad (10)$$

INDUCTANCE.

$$L_1 = \mu\frac{a}{b} = \mu\frac{1}{f} \qquad (11)$$

Note that the same geometrical factor occurs in each case. This useful result holds not only in the case of parallel plate geometries, but is true in general.

We can now calculate Z_o and c.

(i) $$Z_o = \sqrt{\frac{L_1}{C_1}} = \sqrt{\mu \cdot \frac{1}{\epsilon} \cdot \frac{1}{\epsilon \epsilon}}$$

$$= \frac{1}{\epsilon} \sqrt{\frac{\mu}{\epsilon}} \qquad (12)$$

(ii) $$c = \frac{1}{\sqrt{L_1 C_1}}$$

$$= \frac{1}{\sqrt{\mu \epsilon}} \qquad (13)$$

Let us look first at the result for Z_o. In the parallel plate case we can substitute $\epsilon = \frac{b}{a}$ to obtain $Z_o = \frac{a}{b}\sqrt{\frac{\mu}{\epsilon}}$ (14)

In general we can obtain a value for Z_o by noting the analogy between equations (12) and (9), where we note that the formula for Z_o is the same as that for R_1 except that ρ has been replaced by $\sqrt{\frac{\mu}{\epsilon}}$. This means that we can obtain the geometrical factor by calculating the resistance between the

conductors and multiplying by the factor $\frac{1}{\rho}\sqrt{\frac{u}{\epsilon}}$. In cases where a calculation cannot be made, measurements using resistive paper can be used. Here the conductors are painted onto the resistive paper using conducting paint and the resistance between them measured using an ohmmeter. The equivalent to the resistivity is the resistance between two sides of a square of this paper.

Note also the result of equation (13), which shows that the velocity of a wavefront down a two - conductor system is independent of the geometry (provided this is two-dimensional) and is a property only of the medium in which the conductors are placed.

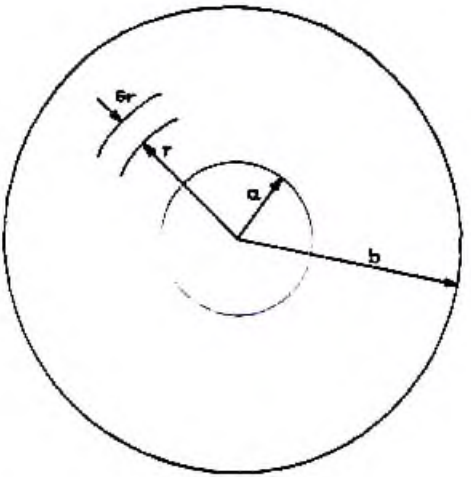
We will now use the results just derived to obtain the impedance of a co-axial line.

IMPEDANCE OF CO-AXIAL LINE

Consider the diagram on the next page. Outwards resistance of co-axial shell at radius r is

$$R(r) = \rho \frac{\delta r}{2\pi r} \qquad (15)$$

Therefore the resistance between inner



and outer conductors for a unit length of cable is

$$R_1 = \int_a^b R(r)dr = \frac{\rho}{2\pi} \int_a^b \frac{dr}{r}$$

$$= \frac{\rho}{2\pi} \ln \frac{b}{a} \qquad (16)$$

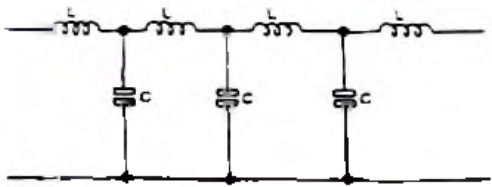
Thus in this case, the geometrical factor

$$f = \frac{2\pi}{\ln \frac{b}{a}} \qquad (17)$$

and therefore the impedance is

$$Z_0 = \frac{1}{\ell}\sqrt{\frac{\mu}{\epsilon}} = \frac{1}{2\pi}\ln\frac{b}{a}\sqrt{\frac{\mu}{\epsilon}} \qquad (1b)$$

which is the standard result for the impedance of a co-axial line.

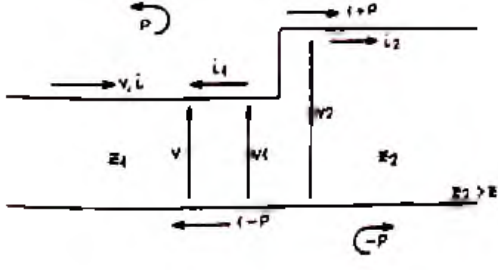


It is common in textbooks to represent a transmission line as shown above. It is possible, on the basis of this model and making use of the Laplace Transform to derive the equations of step propagation. However this method has little to recommend it especially since it appears to lead to a high frequency cutoff which is quite spurious. There is of course no high

frequency cutoff inherent in any transmission line geometry. The only factor which can lead to high frequency cutoff is a frequency dependent behaviour of the dielectric. Clearly, if the dielectric is a vacuum there is no high frequency cutoff.

EFFECT OF DISCONTINUITIES IN TRANSMISSION LINES

Consider a junction between transmission lines of different impedance in the diagram below.



Consider a step v, i incident from the left along line 1. Suppose that this results in two waves at the junction; v_1, i_1 travelling back to the left and v_2, i_2 travelling onward towards the right.

We have, $v = iZ_1$ (19)

Conservation of current (Kirchoff's first law) gives,

$$i = i_1 + i_2 \tag{20}$$

For voltage equality across the junction of the two lines we must have

$$v + v_1 = v_2 \tag{21}$$

Now we have the relations,

$$v_1 = i_1 Z_1 \; ; \; v_2 = i_2 Z_2 \; ; \; v = iZ_1 \tag{22}$$

and (19), (20) and (21) give

$$\frac{v}{Z_1} = \frac{v_1}{Z_1} + \frac{v_2}{Z_2} \tag{23}$$

Substituting $-v_1 = v - v_2$ from (21) into (23) gives: , $\frac{2v - v_2}{Z_1} = \frac{v_2}{Z_2}$

$$\frac{2v}{Z_1} = v_2 \quad \frac{1}{Z_1} + \frac{1}{Z_2}$$

$$2v = v_2 \quad \frac{Z_1+Z_2}{Z_2}$$

Therefore $v_2 = 2v \frac{Z_2}{Z_1+Z_2}$ (24)

Now, since $v_1 = v_2 - v$

$$v_1 = 2v \frac{Z_2}{Z_1+Z_2} - v$$

$$v_1 = v \frac{Z_2-Z_1}{Z_2+Z_1} \quad (25)$$

If we define a reflection coefficient ϱ such that

$$\varrho = \frac{v_1}{v}$$

then $$\varrho = \frac{Z_2-Z_1}{Z_2+Z_1} \quad (26)$$

and we can also write,

$$v_2 = v(1+\varrho) \quad (27)$$

For an incident wave to the right, the relevant coefficients are $-\varrho$ for the reflected wave and $(1-\varrho)$ for the wave continuing to the left.

OPEN AND SHORT CIRCUIT LINES.

If we have a transmission line which comes to a dead end which is an open circuit, we can think of the open as being a line of infinite impedance.

Equation (26) shows that as Z_2 approaches infinity, ρ approaches 1. Thus the step is reflected from the open circuit without inversion. This means that immediately the step arrives at the open it is reflected and adds itself to the voltage already on the line, leading to the familiar doubling effect. It is possible to observe the effect by using an oscilloscope with an input impedance much greater than the line impedance.

Consider now a line which ends in a short circuit, i.e. $Z_2 = 0$. In this case $\rho = -1$, and the step is reflected with inversion so that no voltage is seen at the shorted end. This is hardly surprising since it is a short circuit.

TERMINATION OF LINES.

We see that in both cases considered above, the step was reflected back into the line without loss of energy. In practice, when we interconnect

logic this is an undesirable effect. We would like the step to be perfectly absorbed at the receiving end of the line so that it will have no further consequences.

We see how to achieve this if we note that the mathematics relating to the discontinuity in the line can still be carried through if Z_2 is replaced by a resistor. If we now adjust the value of the resister to be equal to Z_1, we see that $\rho = 0$ and there is no reflection. In a sense there is now no discontinuity in the line and the step behaves as though it were traversing an infinitely long line, i.e. it disappears!

POWER LOSS AT A DISCONTINUITY.

We will consider a step traversing from a line of impedance Z_o to one of impedance $2Z_o$.

In this case, $\rho = 1/3$

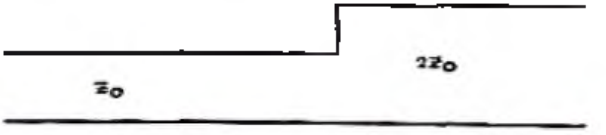
If the incident step is of voltage V, its power is $\frac{V^2}{Z_o}$.

Beyond the change of impedance, the voltage of the step increases to

$v(1+\rho) = \frac{4v}{3}$ and the power becomes $\frac{16v^2}{9} \cdot \frac{1}{2Z_o}$

That is, 8/9 of the power continues on to the right and only 1/9, or 11%, is reflected back. We notice that after the discontinuity the voltage is increased and the current decreased. The discontinuity therefore behaves as a rather lossy transformer.

In practice, Z_o is only a slowly varying function of the geometry of the line, and hence even quite large variations in the geometry load to insignificant reflections.



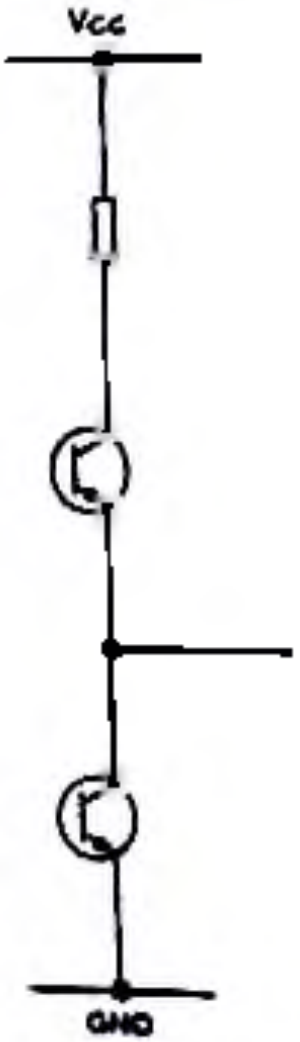
TRANSMISSION LINE THEORY APPLIED TO LOGIC INTERCONNECTION

We have seen in the previous section that the interconnection between logic gates should be viewed as a transmission line and have examined the properties of such lines. We will now look at the sort of device which would be ideal for driving and receiving pulses on such a line, and then consider how closely the available logic families approach this ideal.

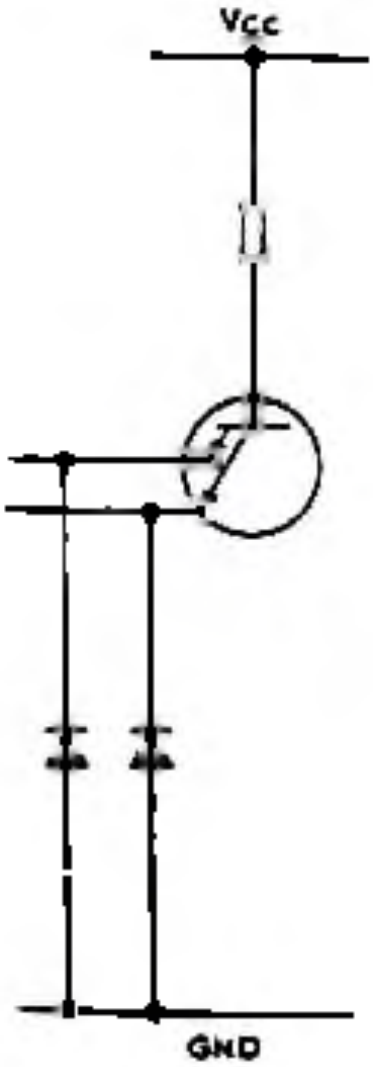
It is assumed in this section that we are dealing with high speed logic, and that the reduction of unnecessary delays is our prime requirement.

TRANSMISSION LINE DRIVING.

We have already noted that, in order to avoid reflections, a transmission line should be terminated in its characteristic impedance. We will examine the implications of this consideration in the case of t.t.l. (transistor-transistor logic). The operation of the basic t.t.l. gate is described elsewhere. Here we will only look at its input and output circuits.



OUTPUT

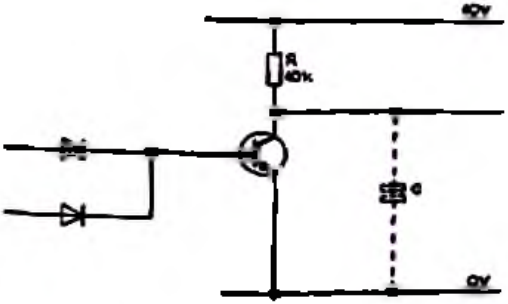


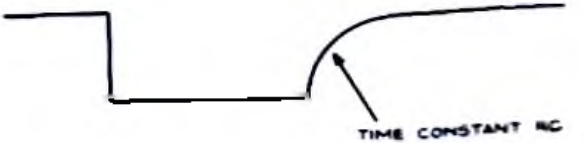
INPUT

HISTORICAL SUMMARY.

Before considering the t.t.l. circuit in detail we will spend some time considering the evolutionary process which led up to it.

In early d.t.l. (diode-transistor logic), transistors were only capable of sustaining 1 mA collector currents. This led to the circuit arrangement shown below where a 10 kohm resistor was used. The circuit shown is clearly a NOR gate, which was the basic d.t.l. element.





One of the problems noted in practice with this circuit was its inability to drive stray capacity. Consider the output waveform above which is obtained when a pulse is applied to the input.

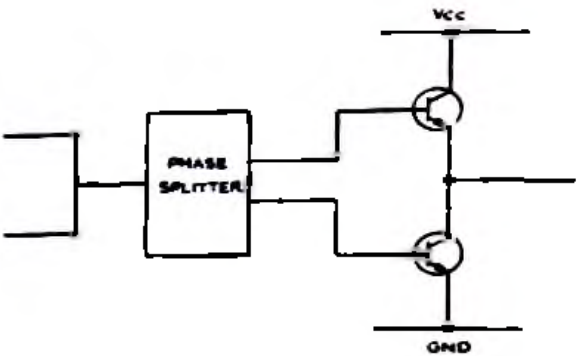
When the transistor switches on the stray capacitance C is discharged through the saturated transistor which offers an impedance much less than 10 kohm; the falling edge is therefore very rapid. The rising edge, however, presents a different picture. Here the transistor switches off and is unable to supply current to charge the stray capacitance through the reverse-biased base-collector junction. This means that the stray capacitance must be charged through the 10 kohm resistor,

leading to an exponential rise which corresponds to a time constant of RC. This is clearly unacceptable as it means that the gate is very poor at driving long signal lines.

Let us, however, recall that in practice the load is not strictly capacitive, but is in fact a transmission line of characteristic impedance around 100 ohms. It is then instructive to ask whether this makes any difference to the conclusion. The answer is that it makes no appreciable difference in this case because R is much greater than 100 ohms; in this limit the capacitive model is quite good.

Designers of logic families tried to circumvent this problem with a two-way 'push-pull' output stage which

N.B. Information on crosstalk between logic interconnections is available in I. Catt, "Crosstalk (Noise) in Digital Systems," IEEE Trans. Electronic Computers, vol. EC-16, pp 743-763, Dec '67



would give rapid transitions in both directions.

They ended up with a totem pole circuit driven by a 'phase splitter' (terrible misnomer) which would ensure that the top transistor was on for a high and the bottom one off, and vice versa. One should clearly avoid the disastrous situation of having both transistors turned on simultaneously. This leads to a very low impedance being placed across the supply rails. In practice, it is difficult to avoid this happening and so one tends to get an overlap of a few nanoseconds when both transistors are on, leading to a

current spike demand from the supply.

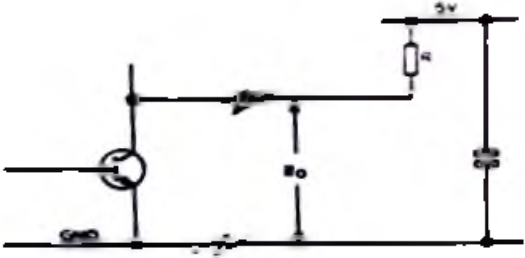
The type of output circuit just described was in fact employed in 73 series logic. This family was not popular - the reasons should be obvious. Because there is no series resistance except that inherent in the semiconductors themselves, the current transients are considerable.

So, the final step in the evolution of t.t.l. was the insertion of a series limiting resistor in the collector of the upper transistor, leading to the output configuration familiar to us all.

Unfortunately, the history of the subject has gone away from a 'straight and narrow' path because, in the evolution of t.t.l., insufficient account has been taken of the way impedance levels and device speeds have changed. Thus, while d.t.l. was working initially with a 10kohm output impedance, we now have t.t.l. devices where the internal pull up resistor is of the order of 100 ohms. The implication of this is that, while with the higher resistance it was permissible to consider the output as being capacitively loaded, with 100 ohm

resistance values this is no longer a sensible model. In fact, since the output load is a transmission line with a characteristic impedance of around 100 ohms, we can no longer neglect its behaviour by lumping the connection and calling it a capacitor.

In fact, it turns out that when we model the interconnection as a transmission line, the upper transistor in the t.t.l. totem pole is redundant and serves no useful function! This is a startling conclusion and takes a little digesting, but if we work through an example, the implications should become clear.



(Serious hazards arise if tri-state t.t.l. is used. See WIRELESS WORLD, June 1978, page 62.)

OPEN-COLLECTOR GATE DRIVING A TRANSMISSION LINE.

The transistor in the diagram opposite could be (and normally would be) the output transistor of a t.t.l. open-collector gate. It is usually thought that the main function of these gates is to provide a wire AND facility in applications where speed is not particularly important; but more of this later.

The transistor is connected to a transmission line of impedance Z_0 and has a pullup resistor R to +5v at the far end. From the point of view of signals, this R shunts the line and therefore, as we have seen earlier, any step arriving at R will not be reflected.

We will now consider what happens when the transistor switches on and off.

(a) Turn-on. When the transistor is off there is no current through R, and therefore the signal conductor is at +5v. When the transistor turns on, its collector voltage falls rapidly to less than 1v. The time taken for this depends on the logic family, but it could be as short as 1 nsec. We will assume

for a moment that whatever this time is, it is much less than the time taken for a step to traverse the line.

After the transistor has switched, a current/voltage step travels along the line. If the voltage step is 4v, the transistor will sink a current given by $i = 4/Z_o$. When the step reaches the receiving end it will be exactly the right size to draw the same current i through the resistor R if we make $R = Z_o$. This is another way of saying that the line is perfectly terminated. After this, nothing else happens until the transmitting gate is again switched on.

(b) Turn-off. This is the more subtle case and seems to be hard to think about, probably because we are happier thinking in terms of voltages than of currents.

We will assume that the transistor turns off very rapidly. This means that the current now has nowhere to flow and a voltage step propagates along the line carrying the message that the transistor

has turned off and current is no longer required! The size of this voltage step is given by $v = iZ_o$, and since i was $4/Z_o$, we get a 4v step. When this step reaches the receiving end of the line, it exactly cancels the voltage across the resistor, and the current flow stops.

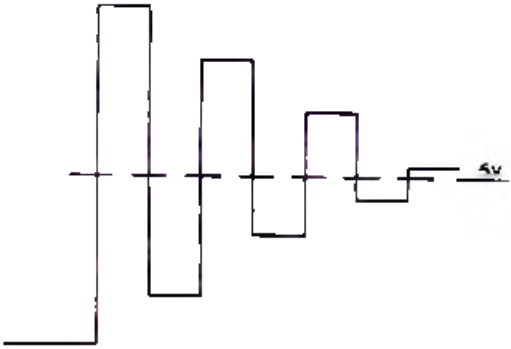
Thus we see that no active pullup is necessary; open-collector gates will quite happily act as line drivers.

Someone is sure to object that they have observed the waveforms at the output of open-collector gates giving the 'normal' exponential rise type of behaviour, and they are quite correct! The point is that if R is far greater than Z_o, the behaviour of the system approximates more and more to what one would expect if the interconnection were replaced by a lumped capacitor. This is simply because since the line is unmatched, the step must make several traverses of the line before it reaches 5v. In other words, the receiving end behaviour is the staircase drawn overleaf. If this staircase is seen on an oscilloscope of

restricted bandwidth, this will be smoothed to give the appearance of the second waveform above; a 'capacitive' behaviour.

Thus, in order to obtain fast settling of the line, we must have R approximately equal to Z_0.

It is worth noting that if R is far smaller than Z_0 we obtain something which approximates to 'inductive' behaviour, with an output waveform shown on the next page.



PRACTICAL CONSIDERATIONS.

There is a practical problem when we come to implement line drivers using open collector gates. This is that an average open-collector device is unable to sink the current it is required to when its output is pulled up to +5v by a resistor of around 150 ohms (the sort of Z_0 one encounters in twisted pairs for instance).

There are two solutions to this and in some cases both must be applied.

(i) Use devices with high sink current capability such as the 7417, 7438 or 74S38.

(ii) Do not pull up to +5v but only to about +3v. This has the effect of slightly degrading the high level noise immunity, but is usually acceptable.

Slightly over-terminate.

If the second course is adopted, it is not necessary to provide a separate power supply. Simply terminate the line with two resistors, R_1 to +5v and R_2 to ground. These resistors are then chosen so that their Thevenin equivalent network has a voltage generator of +3v and an impedance equal to Z_o.

By considering the open circuit voltage and short circuit current it is easily seen that,

$$V_T = 5 \cdot \frac{R_2}{R_1+R_2}$$

$$\text{and } R_T = \frac{R_1 R_2}{R_1+R_2}$$

where V_T and R_T are the Thevenin equivalent voltage and resistance respectively.

BUS DRIVING WITH OPEN-COLLECTOR GATES.

A common requirement in a logic system is to provide a common bus which can be driven at several points and which can provide outputs at several points along its length. We will now consider how this facility can be provided using open-collector devices.

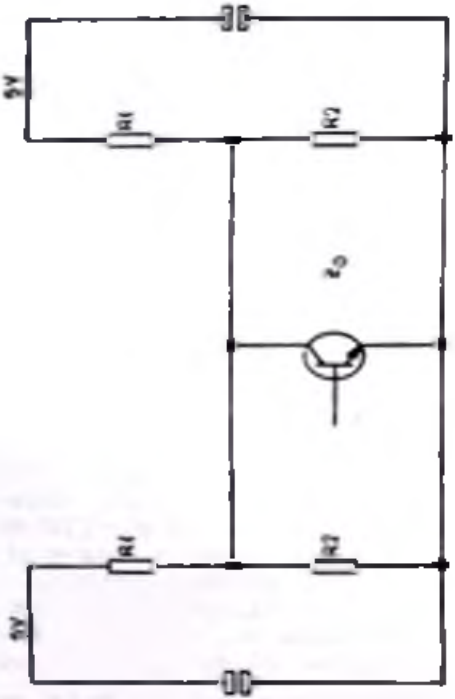
The open-collector device was, until recently, the preferred type for common bus systems but it has recently fallen into disfavour to be replaced by the tri-state type of chip. This is a retrograde step.

The open-collector device fell into disfavour unnecessarily. As we have seen, it is quite capable of driving transmission lines, and does not need the 'crutch' of the upper transistor to obtain rapid switching times.

We will consider a single conductor which forms part of a bus and see how we would go about driving signals along it. (See diagram on next page.)

For the sake of convenient working, we will assume that Z_o = 100 ohms. The values may be scaled to suit any other value of Z_o.

The driving gate, of which only one is shown, is in fact loaded by two


DC
9V
R1
R2
Q
R1
R2
9V
DC

transmission lines going off in each direction. Provided there is no interaction between the lines (which there is not in this case since we assume they go out in opposite directions), the driving gate will 'see' an impedance of Z_o in parallel with another Z_o making 50 ohms.

We will have to terminate the bus at each end so that there will be no further reflection of any signal arriving there. However, since it is difficult to sink the current which such a low termination will inflict on the driving transistor, we will terminate such that R_T is about 10% bigger than Z_o. We will look at the implications of this later. We will also terminate to an effective voltage of -3 volts.

Thus, we have,

$$V_T = 3 = 5 \cdot \frac{R_2}{R_1+R_2}$$

$$R_T = 110 = \frac{R_1 R_2}{R_1+R_2}$$

from which it follows that,
$R_1 = 180$ ohms; $R_2 = 270$ ohms.

We must now calculate the current which the open-collector gate will sink. In the low state there is a maximum of 5 volts across R_1 which gives a current of 28 mA. Since there are two resistors, one at each end, the total current is almost 60 mA. This is quite a high current, although there are devices available which can supply it. It is also quite permissible to use two lower-current devices in parallel.

Clearly, this bus can be driven at any point, and an output obtained from any point.

We remember that we overterminated the bus by 10%. This leads to a reflection of

$$\frac{110 - 100}{110 + 100}$$ i.e. about 5%

which we can safely ignore. In general a mismatch of x% leads to a reflection (voltage) of ½x% if x is small.

We must now consider the effect on our transmission line model of connecting other driver and receiver devices to the bus.

Providing the connecting stubs of these other devices are kept short; less than 10 cm for Schottky t.t.l.

or less than 30 cm for standard t.t.l. we can consider their effect as capacitive and, in fact, they merely lower the characteristic impedance of the bus;

since $Z_o = \sqrt{\frac{L}{C}}$ and we are increasing C.

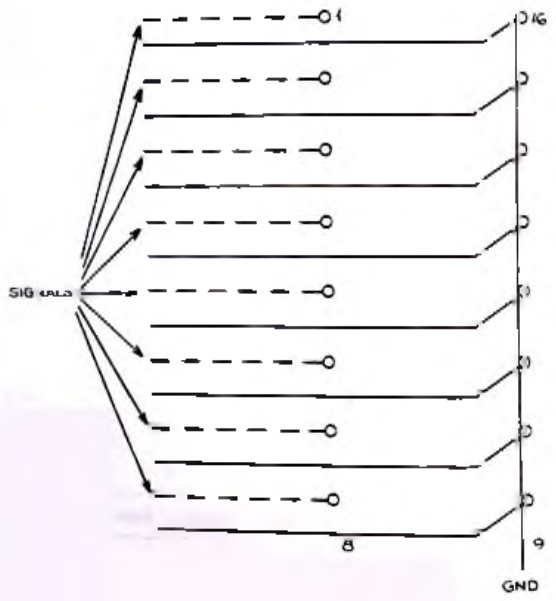
The connections should, however, be kept as short as possible.

In most cases (e.g. twisted pair or printed backplane), Z_o will be greater than 100 ohms and we will not require such 'meaty' drivers as in the example given.

USE OF FLAT MULTIWAY CABLE FOR LOGIC INTERCONNECTION

Many manufacturers (e.g. 3M, Ansley Berg(Du Pont)) are making a flat cable system with crimped connectors which is in many ways ideal for bussing signals around a logic system provided some simple rules are followed.

(i) Use the cable with alternate conductors grounded. This means that on a 16-way cable you would only send 8 signals. (+5 volts would of course do just as well as ground.) If the cable is terminated in a standard 16


1
16
SIGNALS
8
9
GND

pin DIP plug and socket it is simple to carry out this grounding since alternate conductors are brought out to opposite sides of the plug as shown in the diagram opposite.

One of the manufacturers (Ansley) is introducing a cable with conductors on half the pitch (0.025 instead of 0.050 inch). They are also introducing a connector which automatically grounds alternate conductors via a single pin. This new cable will represent a useful advantage in reduced size.

(ii) Terminate correctly. There is a slight subtlety which you will notice if you refer back to the diagram opposite. All the signal conductors except one have a ground at each side of them - so we are dealing with two signal impedances.

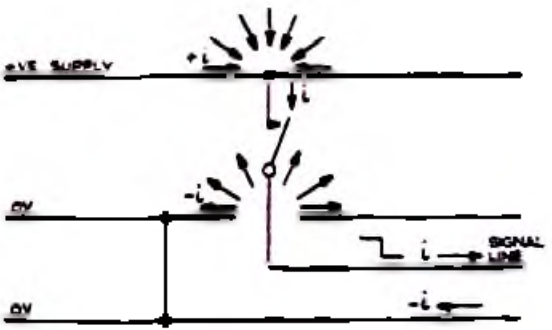
For 'Scotchflex' Cable (3M) the edge conductor has an impedance of 140 ohms while those in the centre have an impedance of 110 ohms.

It is suggested that all signal lines be terminated in 140 ohms. This will give about 12.5% reflection on seven of the lines which is acceptable. Alternatively a compromise figure about halfway

between the two values can be chosen. One of the advantages about transmission lines in logic is that you only have to approximately impedance match.

LOCAL DECOUPLING OF VOLTAGE SUPPLIES BY PRINTED CIRCUIT VOLTAGE PLANES

When a logic gate switches on, a signal is launched down the signal line, the current step i being taken from the +ve supply line, and an equal and opposite current -i being dumped into the 0v line at the point where the logic signal originated.

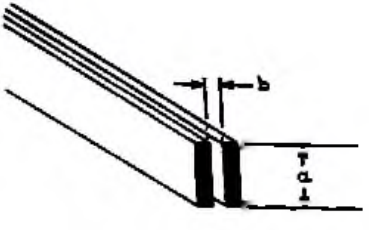


As a result, in order to satisfy Kirchoff's Law that the total current at any point must be zero, a circular wave of current and voltage - like the ripple caused by a stone dropped into

a pond flows out between the +ve supply voltage plane and the 0v plane. It is important that the impedance seen by such a signal flowing out between the voltage planes, which can be regarded as a source impedance of the logic signal, should be small. Otherwise the +ve voltage difference between the two planes at the signal source will temporarily collapse.

THE PIE SHAPED TRANSMISSION LINE

In order to understand the nature of the decoupling action at a point between parallel voltage planes, it is easiest to approach it by way of the parallel plate transmission line and the pie shaped transmission line.

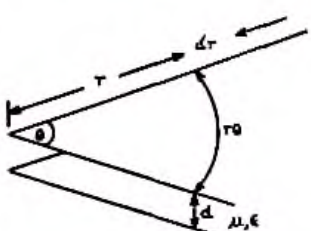


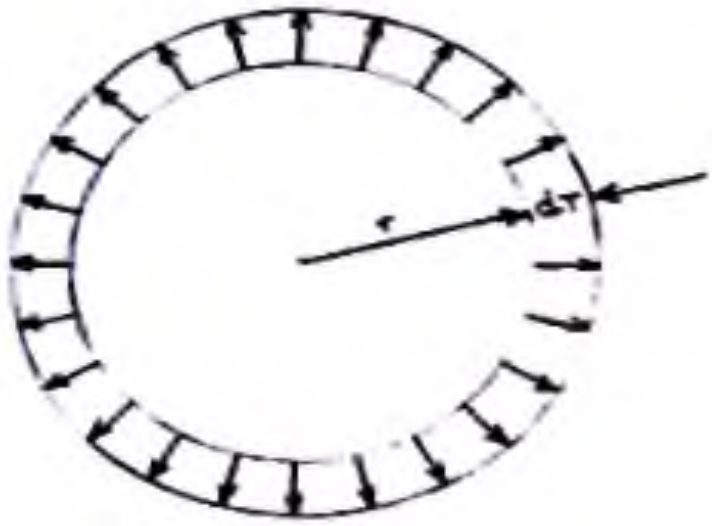
The formula for the characteristic impedance of a parallel plate transmission line of width a and separation b with negligible fringing at the edge (because a is much bigger than b) is

$$Z_o = \frac{b}{a}\sqrt{\frac{\mu}{\epsilon}}$$

This formula still applies for each small section of a transmission line where the width a is varying, in particular for a pie shaped transmission line, where over a distance δr it becomes

$$Z_o = \frac{d}{r\theta}\sqrt{\frac{u}{\epsilon}}$$





Now if $\theta = 2\pi r$, that is, we are considering a complete plane, we get

$$Z_0 = \frac{d}{2\pi r}\sqrt{\frac{\mu}{\epsilon}}$$

Now we know that in a medium with permittivity ϵ and permeability μ, the outwards velocity of the signal must be $\frac{1}{\sqrt{\mu\epsilon}}$

Therefore the velocity, $c = \frac{r}{t} = \frac{1}{\sqrt{\mu\epsilon}}$

where time t is the time since the signal was introduced at the centre.

So using this last equation to substitute for the distance r we get;

$$Z_o = \frac{d\,\mu}{2\,\pi\,t} \quad \text{ohms},$$

where d is in metres.

A reflection related to Z_o arrives back at the centre at time 2t. If Z_o is small when $2t = t_r$ (the rise time of the output of the logic gate), then natural decoupling between planes is satisfactory.

As an example, if $2t = 1$ nsec, $d = 0.5$ mm, $\mu = 4\pi \times 10^{-7}$,

$$Z_o = \frac{0.5 \times 10^{-3} \times 4 \times 10^{-7}}{2\pi \times \frac{1}{2} \times 10^{-9}} = 0.2 \text{ ohms}$$

This calculation shows that it is possible to keep the decoupling between voltage planes satisfactory by the addition of extra decoupling capacitors distributed at intervals of a few centimetres, to prevent superposition of signals from generating unacceptably large voltage transients between planes.

The proportion of the surface area occupied by the miniature tantalum capacitors will be insignificant.

DIGITAL ELECTRONICS NEEDS SOUND THEORY

The digital electronics industry has sprung up so quickly in the past few years that the theoretical foundation required has not developed at all. It is impossible to cross the line separating the analogue and digital worlds. The sine wave is a periodic, time varying, steady state phenomenon, whereas a digital signal is a fixed amplitude step (shock wave). Each change of state is a single event in time and cannot be correlated with any other change. A dubious connection via Fourier Analysis, is merely a mathematical arpeggio, guaranteed to be worth a few exam questions at least. The leading edge of a step is a shock wave; it is a transverse electromagnetic wavefront (T.E.M.) which travels at the speed of light. Of course, it might be possible to create this single step using Fourier Analysis, but this would mean combining an infinite number of sine waves which exist from minus infinity to plus infinity. This can easily be seen to be quite absurd and of no practical use.

The hard and fast rules laid down for periodic sine waves must be cast aside and new rules developed for the shock wave. An obvious area to concentrate on is signal distribution. We must have a basic understanding of the mechanism by which a block or pulse of energy is transmitted in space. This leads us into electromagnetic theory, and it is here that the student will learn and ultimately understand the subject of digital electronics.

Unfortunately, nearly all the books written on electromagnetic field theory are concerned with steady state sine waves. There is no basic theory written today which concentrates on high speed digital techniques. How ins steps propagate is known to only a few people. Yet with the advent of emitter coupled logic (e.c.l.) and Schottky t.t.l., this electrical phenomenon is becoming widespread. Engineers today attempt to put together fast, complex logic systems which stand the risk of failure. The paper design might well be satisfactory, but the problems that arise during testing and commissioning seem endless. The unfortunate engineer just cannot understand the "gremlins" that keep upsetting his system.

Nowhere is he taught the important fundamental principles necessary for competent digital system development.

To have a complete understanding of high speed systems, one must apply certain techniques which are not taught in any educational establishment in the country, nor written about in any text book. One must go back to the turn of the century to find any suitable material. Then, the main subject was telegraph signalling, which is analogous to digital transmission today. A 10 millisecond rise time step travelling 1,000 kilometres (telegraphy) is based on the same theoretical principles as a 1 nanosec. step travelling 10 centimetres (computers).

Around 1890-1910, Oliver Heaviside and his contemporaries - Oliver Lodge, S.P. Thompson and Hertz developed many theories which should be used today. By thinking of digital signals as small, discrete packets of "energy current" flowing at the speed of light between the wires (which merely act as a guide), many of the present day design implementation problems could

be solved. The advent of the telephone and wireless led to the predominance of sinusoidal time varying signals, so the concept of "energy current" was lost as new theories were developed to cope only with the periodic waveform. We have now turned a full circle, and must look backwards before we can advance.

The practical problems of digital systems, such as cross talk (noise), power supply decoupling, signal termination and drive techniques, component pulse response, earthing, and mains borne interference, need to be studied. General models and original concepts based upon Oliver Heavisides's "energy current" idea can be used to tackle these problems, making it possible to design complex digital systems in an orderly, scientific fashion. Every practising engineer in digital electronics must stop attempting to use analogue ideas for digital systems; they will not work. Pattern sensitivity, noise, power supply problems are all raising their ugly heads, and all quite unnecessarily. By following clearly defined design rules, systems can be

built which will work reliably and first time, without the usual three to six month commissioning troubles.

The design concepts that are used are not difficult. Although soundly based in theory, they do not involve exotic mathematics, and are aimed specifically at practical problems of hardware development. They are tools of the trade to be used by all engineers and technicians.

ENERGY CURRENT

Oliver Heaviside, who had the advantage of coming later, had a better grasp of electromagnetics than did Faraday or Maxwell, and his view of how a digital signal travels is well worth study.

Whereas the conventional approach to the subject today is to concentrate on the electric current in wires, with some additional consideration of voltages between wires, Heaviside concentrates primarily on what he calls "energy current", this being the electromagnetic field which travels in the dielectric between the wires. In the quotation below, Oliver Heaviside's phrase, "We reverse this;" points to the great watershed in the history of electromagnetic theory, between the "ethereals", who with Heaviside believe that the signal is an "energy current" which travels in the dielectric between the wires, and the "practical electricians", who like

John T. Sprague believe that the signal is an electric current which travels down copper wires, and that if there is a "field" in the space between the wires, this is only a result of what is happening in the conductors.

In his "Electrical Papers", Vol. 1, 1892, page 438, Heaviside wrote;

> Now, in Maxwell's theory there is the potential energy of the displacement produced in the dielectric parts by the electric force, and there is the kinetic or magnetic energy of the magnetic induction due to the magnetic force in all parts of the field, including the conducting parts. They are supposed to be set up by the current in the wire. We reverse this; the current in the wire is set up by the energy transmitted through the medium around it.....

The importance of Heaviside's phrase, "We reverse this;" cannot be overstated for digital designers. It points to the watershed between the

"practical electricians", who have held away for the last half century, promulgating their theory, which we will call "Theory N", the Normal Theory, that the cause is electric currents in wires and electromagnetic fields are merely an effect; and the "etherials", who believe what we will call "Theory H"; that the travelling field is the cause, and electric currents are merely an effect of these fields.

The situation is of course obscured by the many who claim that it is immaterial which causes which. However, experience shows that it is damaging to ignore causality when we are trying to assemble reliable digital systems.

Before continuing with Theory H, we will quote one early Theory N man, a "practical electrician" named John T. Sprague. In his book, "Electricity:Its Theory Sources and Applications", 1892 he ridicules Theory H on page 239;

> A new doctrine is becoming fashionable of late years, devised chiefly in order to bring the now important phenomena of alternating currents under the mathematical

system. It is purely imaginary..., based upon Clerk-Maxwell's electromagnetic theory of light, itself correctly described by a favourable reviewer as "a daring stroke of scientific speculation," alleged to be proved by the very little understood experiments of Hertz, and supported by a host of assumptions and assertions for which no kind of evidence is offered; but its advocates now call it the "orthodox" theory.

This theory separates the two factors of electricity....., and declares that the "current," the material action, is carried by the "so called - conductor" (which according to Dr. Lodge contains nothing, not even an impulse, and according to Mr. O. Heaviside is to be regarded rather as an obstructor), but the energy leaves the "source" (battery or dynamo) "radiant in exactly the same sense as light is radiant," according to Professor Silvanus P. Thompson, and is carried in space by the ether: that it then "swirls" round (cause for such swirling no one

explains) and finds its way to the conductor in which it then produces the current which is apparently merely an agency for clearing the ether of energy which tends to "choke" it, while the conductor serves no other purpose than that of a "waste pipe" to get rid of this energy.

*****

This much, however, is certain; that if the "ether" or medium, or di-electrics carry the energy, the practical electrician must not imagine he can get nature to do his work for him; the ether, &c., play no part whatever in the calculations he has to make; whether copper wire is a conductor or a waste pipe, that is what he has to provide in quantity and quality to do the work; if gutta percha, &c., really carry the energy, he need not trouble about providing for that purpose; he must see to it that he provides it according to the belief that it prevents loss of current. In other words, let theoretical mathematicians devise what new theories they

please, the practical electrician must work upon the old theory that the conductor does his work and the insulation prevents its being wasted. Ohm's law (based on the old theory) is still his safe guide.

For this reason I would urge all practical electricians, and all students who desire to gain a clear conception of the actual operations of electricity, to dismiss from their minds the new unproved hypotheses about the ether and the abstract theory of conduction, and to completely master the old, the practical, and common sense theory which links matter and energy together,.....

Sprague accurately described Theory N, which has been used in practice by virtually every digital designer, with disastrous results. They must now turn to Theory H to get them out of their difficulties.

In his book "Magnets and Electric Currents", 1898, J.A. Fleming argued on page 80 for Theory H;

It is important that the student should bear in mind that, although we are accustomed to speak of the current as flowing in the wire in one direction or the other, this is a mere form of words. What we call the current in the wire is, to a very large extent, a process going on in the space or material outside the wire. Just as we familiarly speak of the sun as rising and setting, when the effect is really due to the rotation of the earth, so the ordinary language we use in speaking about electric currents flowing in conductors retains the form impressed upon it by older and erroneous assumptions as to their nature.

The reader will have surmised by now that "energy current", the primary signal which travels down the dielectric from one logic gate to the next, has an amplitude equal to the Poynting Vector, E x H.

We will end this qualitative discussion with some of the more important quotations from Heaviside,

the man who a century ago brilliantly used the concept of energy current to solve telegraph problems which closely parallel present day problems in high speed digital logic.

In his "Electrical Papers", Vol. I, 1892, page 438, Heaviside wrote;

> It becomes important to find the paths along which the energy is being transmitted. First define the energy-current at a point to be the amount of energy transferred in unit time across unit area perpendicular to the direction of transmission..... This is true universally, irrespective of the nature of the medium as to conductivity, capacity, and permeability,..... and is true in transient as well as in steady states. A line of energy-current is perpendicular to the electric and the magnetic force, and is a line of pressure. We here give a few general notions.
>
> Return to our wire from London to Edinburgh with a steady current from the battery in London. The energy is poured out of the

battery sideways into the dielectric at a steady rate...Most of the energy is transmitted parallel to the wire nearly... But some of the outer tubes go out into space to an immense distance..... If there is an instrument in circuit at Edinburgh, it is worked by energy that has travelled wholly through the dielectric, then finding its way into the instrument,... where it enters ..... and is there dissipated.....

In a circular circuit, with the battery at one end of a diameter, its other end is the neutral point; the lines of energy current are distributed symmetrically with respect to the diameter.

On closing the battery circuit (i.e. switching the logic output) there is an immediate rush of energy into the dielectric...."

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1986 comment. The series now comprises four volumes in the following sequence; DIGITAL ELECTRONIC DESIGN VOL 1, VOL 2, ELECTROMAGNETIC THEORY VOL 1, VOL 2. Please use the cumulative index in the last volume. Also make use of articles and letters in Wireless World almost every month from mid 1978 to the present day, March 1986.

The following associated books are intended for publication in the near future;

A biography of Oliver Heaviside by his friend Searle. (At present, no biography longer than 30 pages exists. The Searle biography is authoritative and totals some 40,000 words.)

The first volume of the collection of articles and letters in Wireless World, those from 1978 to around 1982.

This volume was for a time replaced by DIGITAL HARDWARE DESIGN pub. Macmillan, which has gone out of print, so this volume returns onto the market.

For a recent bibliography, look up References in Wireless World Sep 84 pwd, Nov 85 p36, Dec 85 p75.

March 86. Universities and colleges are now bringing this material into their courses.